AMENDMENTS TO THE CLAIMS

1-16. (Cancelled)

17. (New) A data transfer circuit comprising:

a first latch section that outputs a single-phase first latch result; and

a second latch section that latches said single-phase first latch result,

wherein said first latch section includes a first inverter and a second inverter, an input from said first inverter being inputted to said second inverter via a switching circuit, and

wherein a power supply voltage of said first latch section is raised from a first voltage to a second voltage while said single-phase first latch result is transferred to said second latch section.

18. (New) The data transfer circuit according to claim 17, wherein said second voltage is higher than said first voltage.

19. (New) The data transfer circuit according to claim 17, wherein said second voltage is a power supply voltage of said second latch section.

20. (New) The data transfer circuit according to claim 17, wherein said second voltage is sufficient to prevent a voltage drop due to the transfer of said single-phase first latch result to said second latch section.

21. (New) The data transfer circuit according to claim 17, wherein said second voltage is about 5.8 V.

22. (New) The data transfer circuit according to claim 17, wherein said second voltage is at least 2.9 V greater than said first voltage.

23. (New) The data transfer circuit according to claim 17, wherein said single phase first latch result is an inverted output of the first latch result.

24. (New) The data transfer circuit according to claim 17, wherein said first latch section latches gradation data.

25. (New) The data transfer circuit according to claim 17, wherein said first and second inverters are arranged in parallel between said first power supply voltage and a first negative power supply.

26. (New) The data transfer circuit according to claim 25, wherein data input is inputted to said first inverter.

27. (New) The data transfer circuit according to claim 17, wherein said switching circuit operates off-action at a sampling pulse.

28. (New) The data transfer circuit according to claim 25, wherein said data input is inputted to said first inverter via a transistor that operates on-action at said sampling pulse.

29. (New) The data transfer circuit according to claim 17, wherein a transfer switch is arranged between said first latch section and said second latch section, an output of said transfer switch being supplied to said second latch section.

30. (New) The data transfer circuit according to claim 17, wherein said second latch section further comprises a third inverter and a fourth inverter, said third and fourth inverters arranged in parallel between said power supply voltage.

31. (New) The data transfer circuit according to claim 30, wherein said first latch result is inputted to said third inverter.

32. (New) The data transfer circuit according to claim 30, wherein said second latch section level shifts said transfer circuit output by setting-up said negative power supply.

33. (New) The data transfer circuit according to claim 17, wherein said power supply voltage of said first latch section is raised from said first voltage to said second voltage before said single-phase first latch result is transferred to said second latch section.

34. (Withdrawn-New) The data transfer circuit according to claim 17, wherein said single phase first latch result is a non-inverted output of the first latch result.

35. (Withdrawn-New) The data transfer circuit according to claim 34, wherein said power supply voltage of said first latch section is raised from said first voltage to said second voltage before said single-phase first latch result is transferred to said second latch section.

36. (Withdrawn-New) The data transfer circuit according to claim 35, wherein said second voltage is sufficient to prevent a voltage drop due to the transfer of said single-phase first latch result to said second latch section.